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Nanoelectronic Devices and Integrations on Silicon Platform Today and Tomorrow

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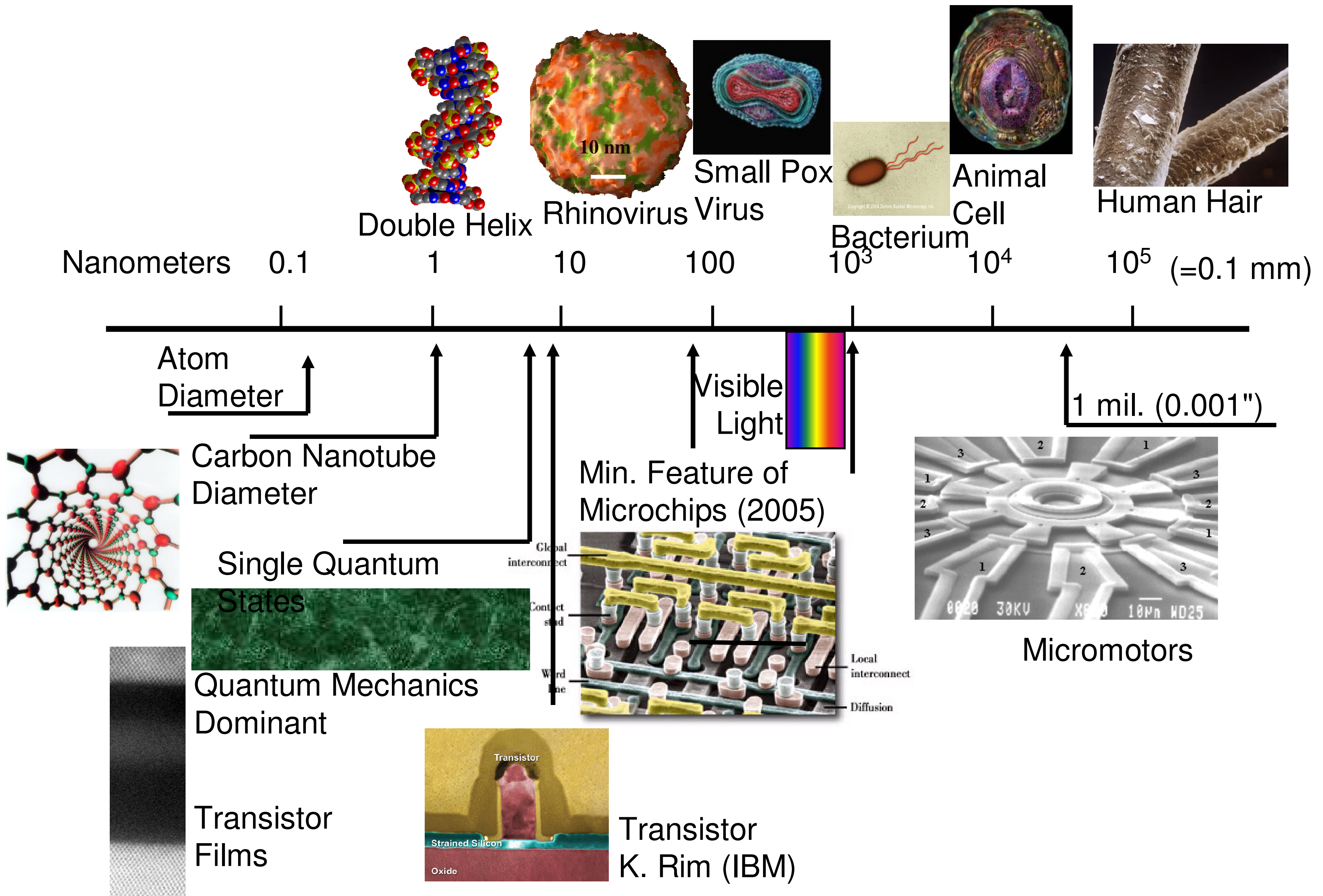
[URL:http://nanodevice.stanford.edu](http://nanodevice.stanford.edu)

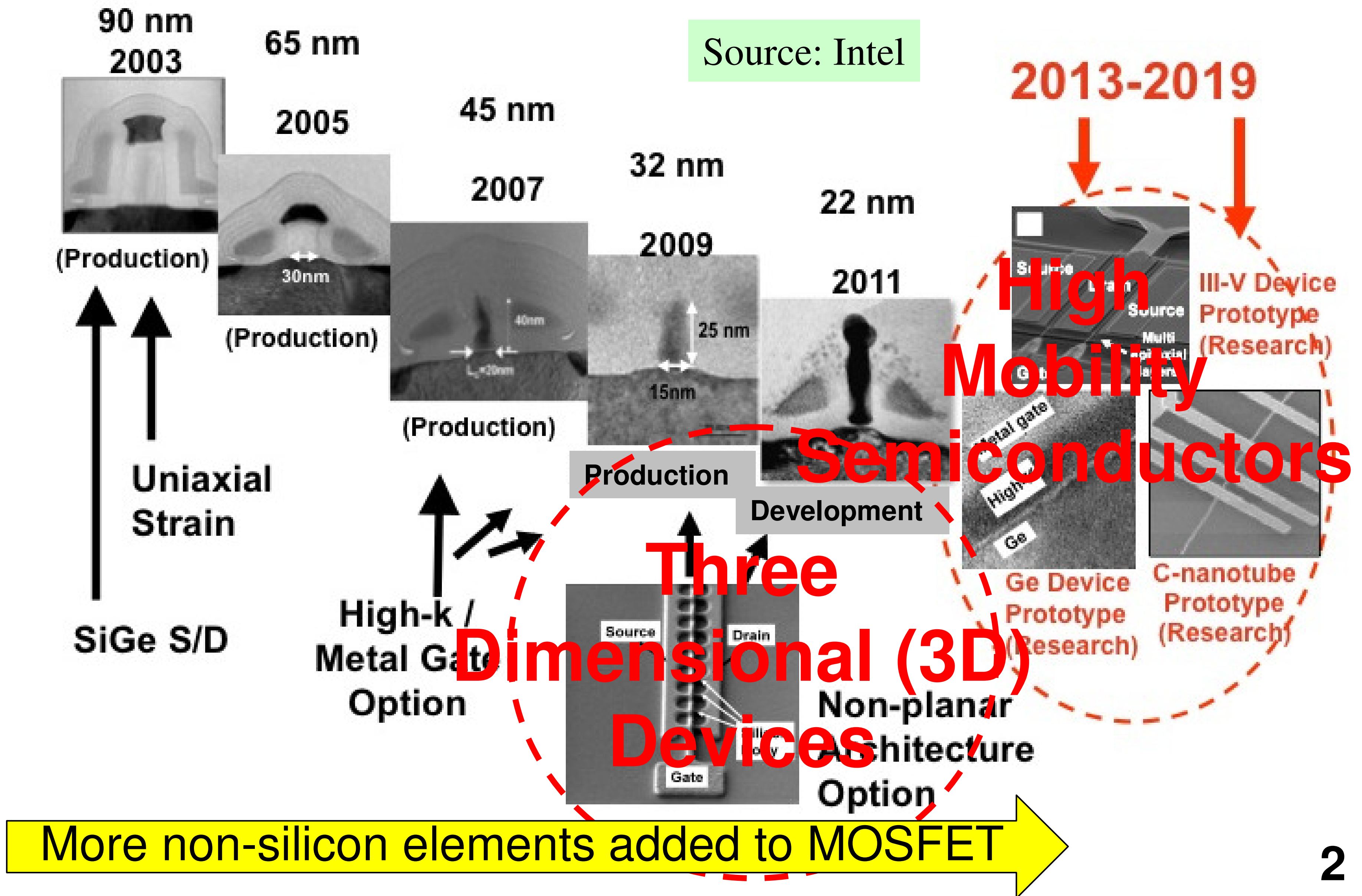
Nanostructure Size Scales



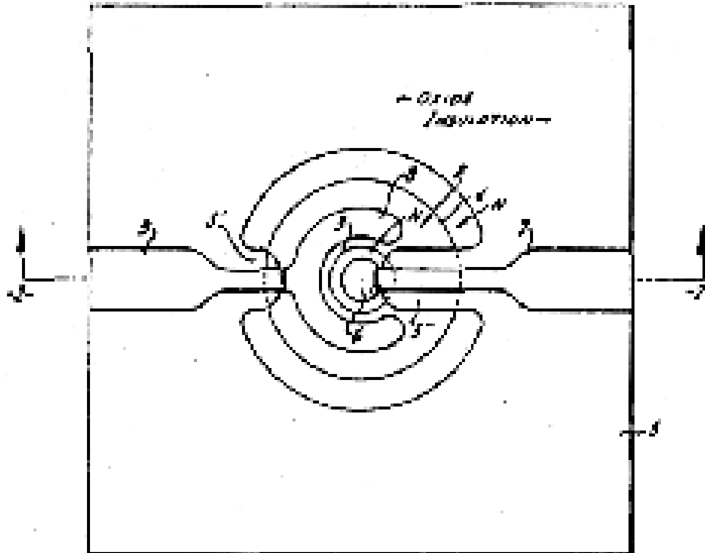
Nanoelectronics at large

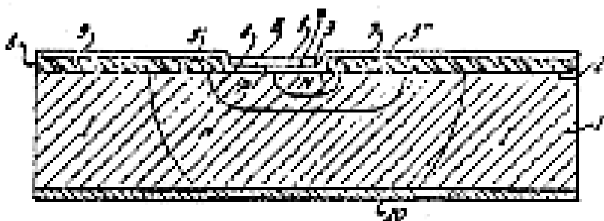
- Evolutionary "nano"
  super scaled CMOS
  beyond silicon but with silicon
  MEMS/NEMS
- Revolutionary "nano"
  nanodots,
  nanowires/nanotubes
  graphene
  organic/molecular
  spintronics
  topological insulator
  new functional materials for nonvolatile memory

Transistor Scaling



1959: 1st Planar Integrated Circuit





Robert N. Noyce

Now non-planar 3-Dimensional Devices?

Germanium to Silicon

John Moll: …..the most dominant reason to switch to silicon was its band gap, i.e. large enough to reduce pn junction leakage, yet small enough to be semiconductor at practical temperature range…and the stable oxide as surface passivation and also as diffusion mask for most of group III and V elements…

Now back to Germanium?

Before going further…

What is our track record in predicting the future?

Roadmap in 1965

- By 1980, Silicon IC (meant bipolar IC mostly) will be replaced by functional device based IC's, i.e. Gunn effect devices
- Non-volatile memory, MNOS, will be replacing magnetic thin film memory.
- Geometry shrink will continue within foreseeable future.

Roadmap in 1976

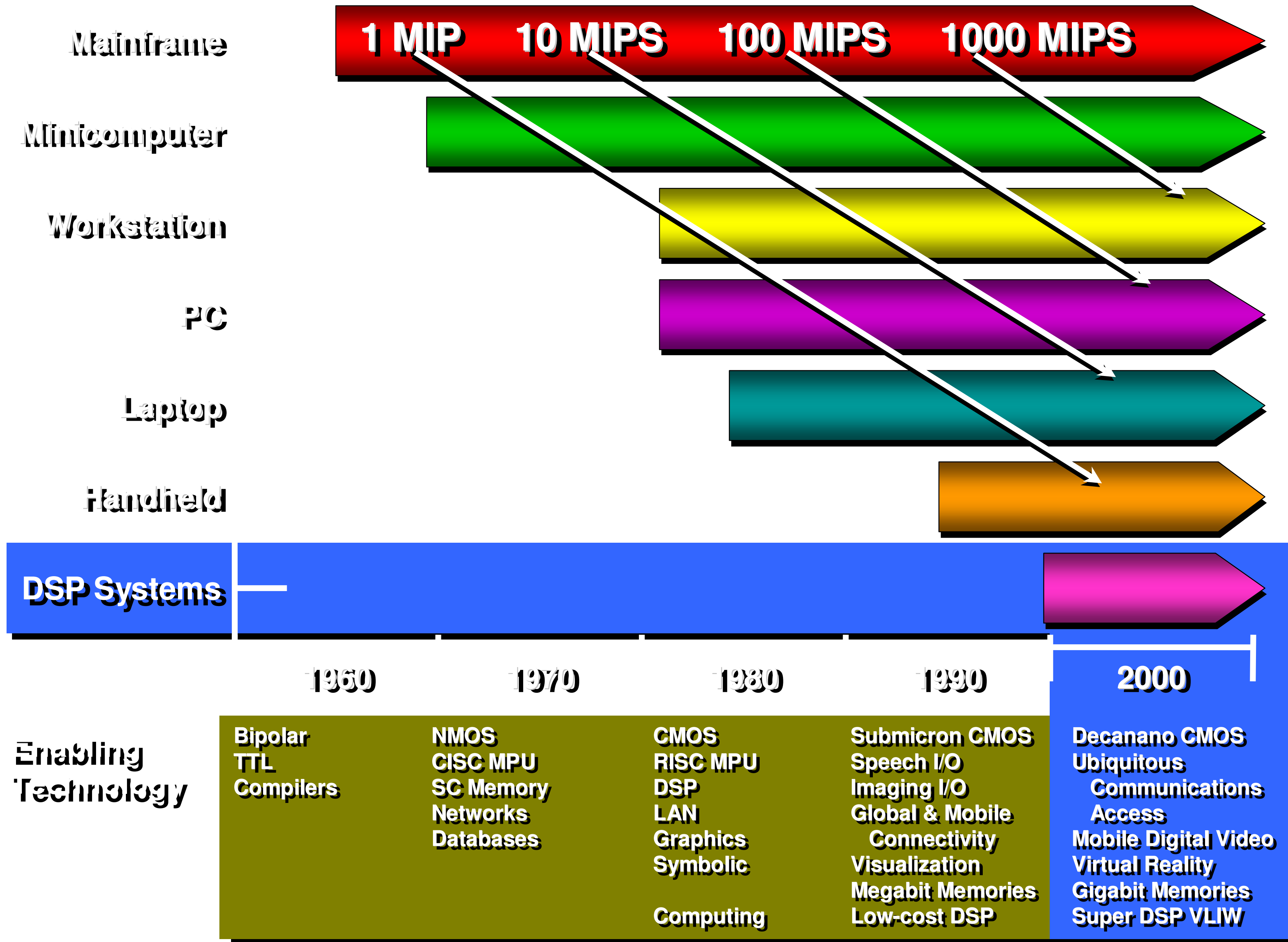
- Optical litho will be replaced by e-beam and/or x-ray circa 1985
- Silicon IC will be replaced by GaAs circa 1985
- Bulk CMOS will be replaced by SOS
- Geometry shrink will continue in .7x in every other year

Even ITRS…..

NTRS to ITRS

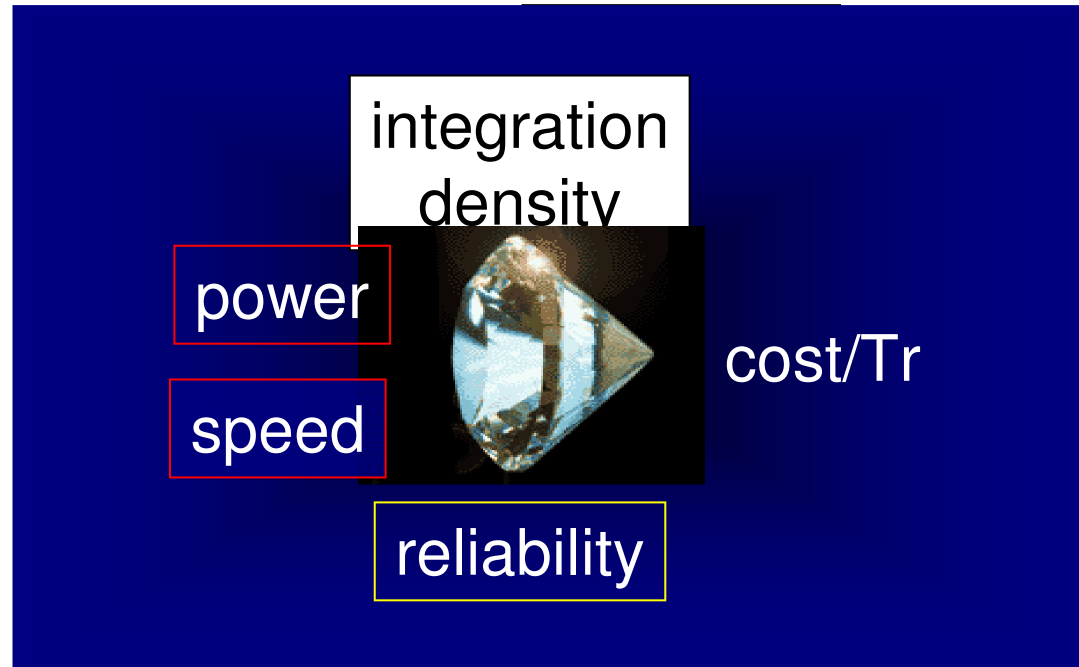
Slipped schedules by 3-4 years only from1994 through 1998!!

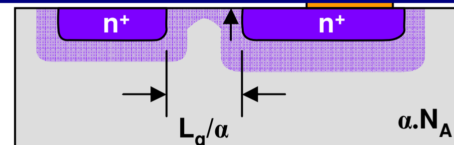
Lately decided to put everything on the table, keep growing pages!


Moving Power to the Person
Mainframe
Minicomputer
Workstation
PC
Laptop
Handheld
1 MIP
10 MIPS
100 MIPS
1000 MIPS
DSP Systems
1960
1970
1980
1990
2000
Enabling Technology
Bipolar
TTL
Compilers
NMOS
CISC MPU
SC Memory
Networks
Databases
CMOS
RISC MPU
DSP
LAN
Graphics
Symbolic
Computing
Submicron CMOS
Speech I/O
Imaging I/O
Global & Mobile Connectivity
Visualization
Megabit Memories
Low-cost DSP
Decanano CMOS
Ubiquitous Communications Access
Mobile Digital Video
Virtual Reality
Gigabit Memories
Super DSP VLIW

The happy scaling: for how long?

R. Dennard © IEEE





dimensions t_{ox}, L, W	$1/\alpha$
doping	α
voltage	$1/\alpha$
integration density	α^2
delay	$1/\alpha$
power dissipation/Tr	$1/\alpha^2$

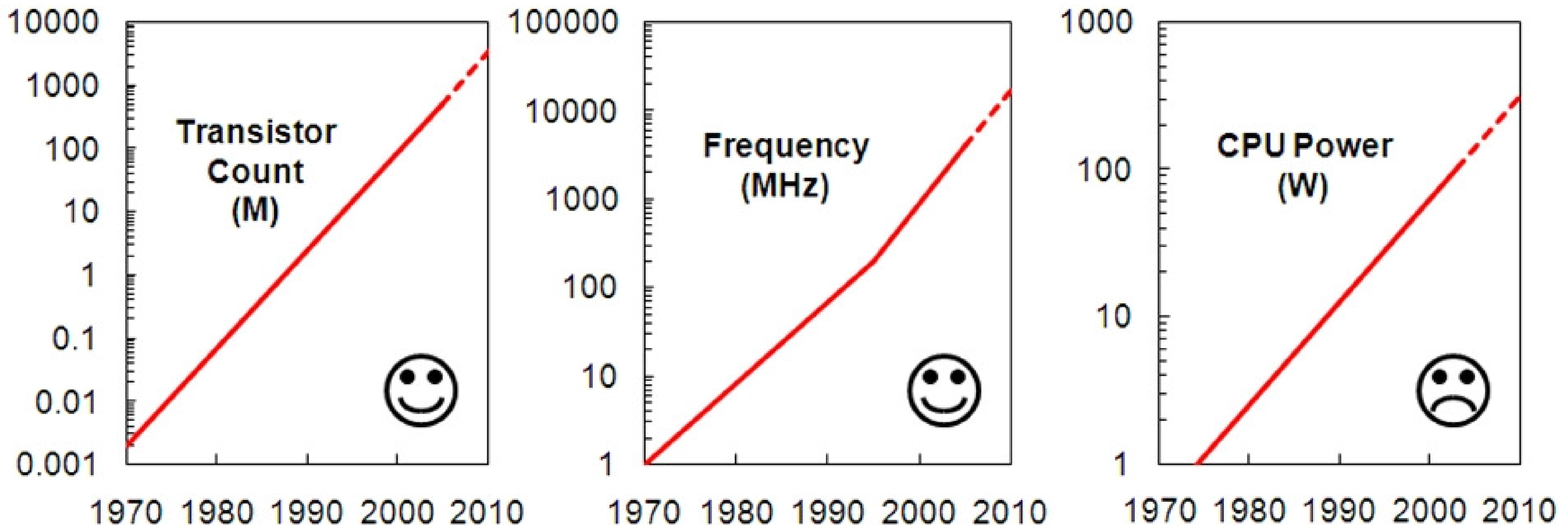
Smaller = better

M. Brillout, FTM2006

…However,….

Microprocessor Trends

Higher Transistor Count x Higher Frequency = Higher Power

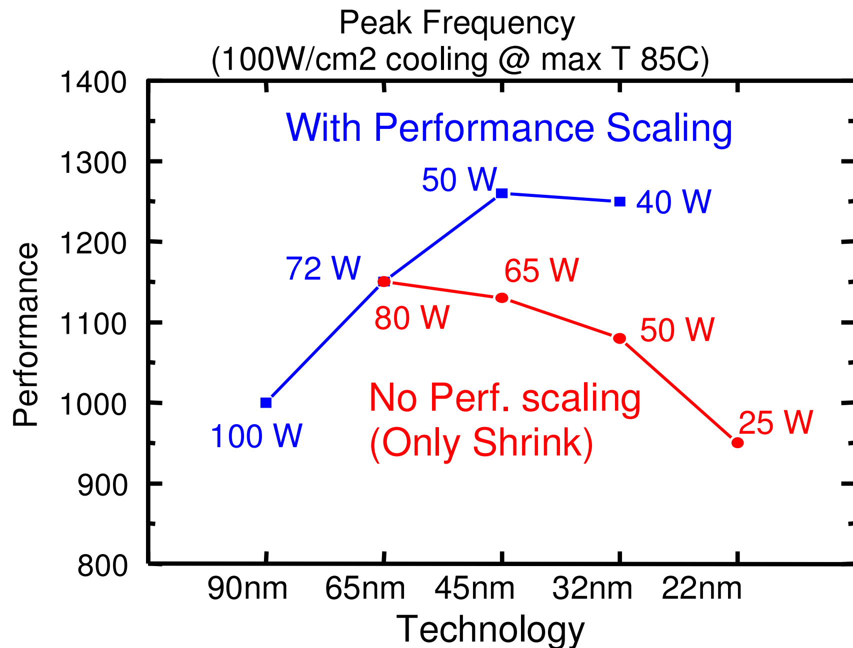


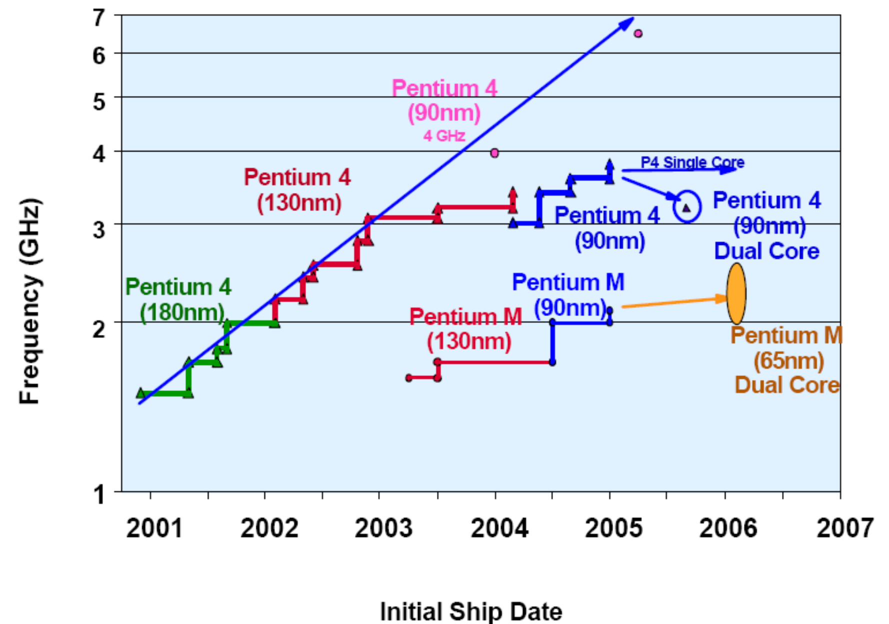
Moore's Law hits the power wall

Mark Bohr, EE310 seminar at Stanford 2011

Paradigm Shift: Hitting the Cooling Limit

- Moving a high power chip to the next node (with limitation on cooling and maximum T rise), actually will slow it down





End of frequency scaling @ ~4 GHz (with 100 W cooling)?

Today

Changed vs Unchanged

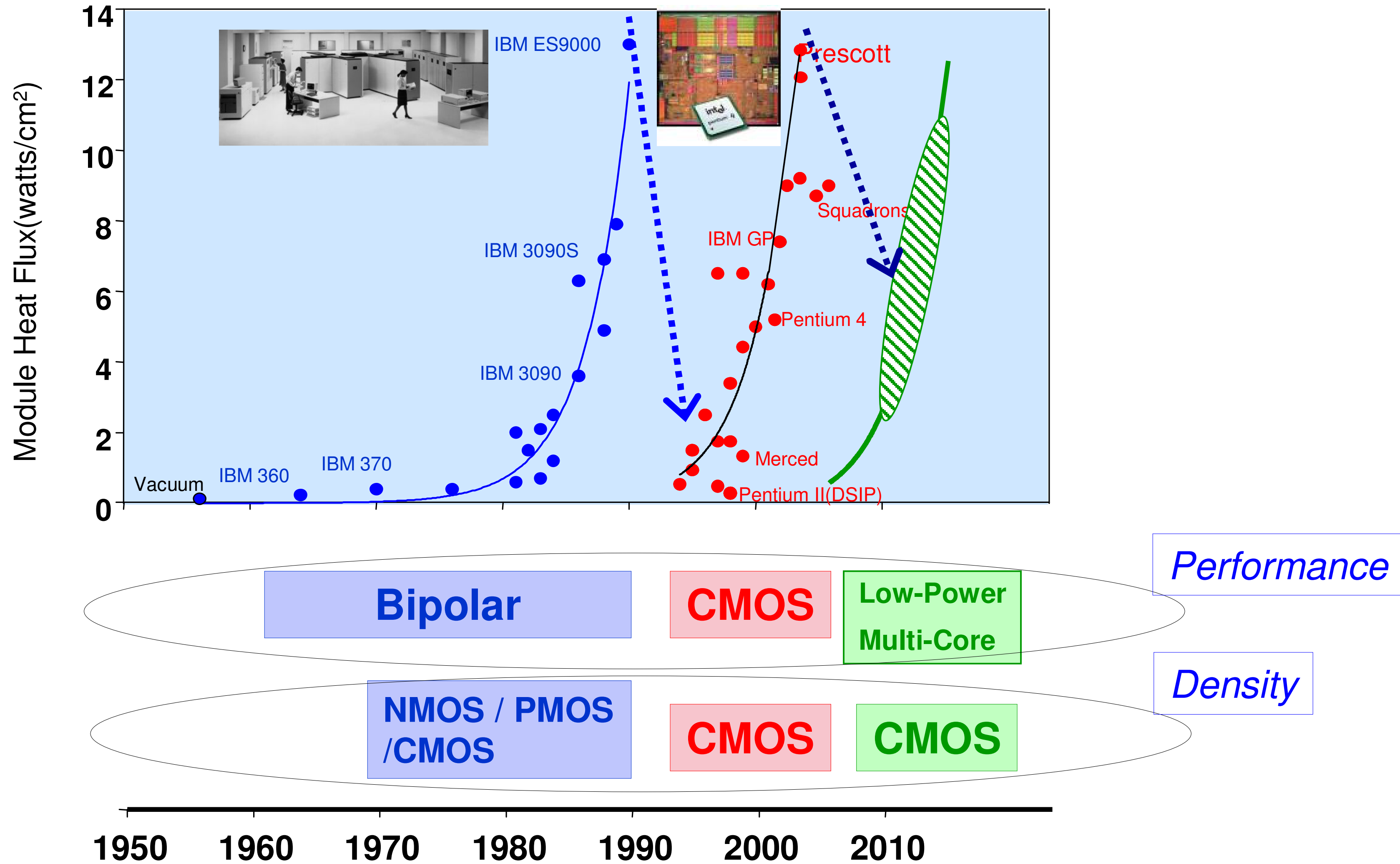
- Scaling down continues, but is closer to the limit
- Driving force switched from “faster clock” to “less power consuming”
- All kinds of “nano” opportunities in evolutionary nano and revolutionary nano.
- Paradigm change for acceptance of “uncommon” materials
- Variety of new applications in non-traditional field, i.e. bio-, medical-, sensing-…

…..Let’s take a look….

Can we reduce power consumption at system level?

- Introduction of multi-core system to suppress the needs for aggressive clock frequency
- 3 D integration at package level, die level.wafer level, monolithic 3D…..
- Interconnect

System Performance from Multi-Cores, as simple scaling cannot deliver solution



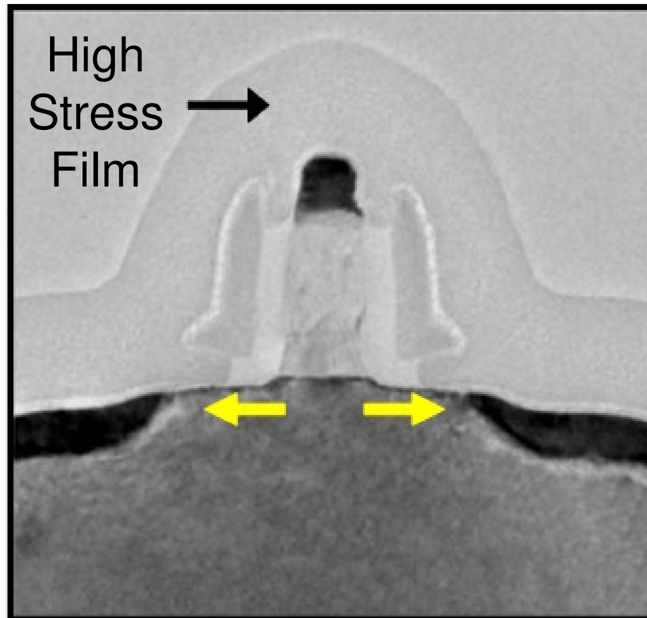
G. Shahidi, IBM, at ITPC 2007

Can we further reduce power consumption at individual device level?

- Better electrostatics: Steeper sub-threshold slope by FDSOI, double gate FET, Trigate/Fin FET, Tunnel FETs………
- Better carrier transport: Power supply voltage reduction by higher mobility channel
- DIBL/GIDL reduction: Source/drain/channel engineering and optimization
- Non-volatile memory and logic

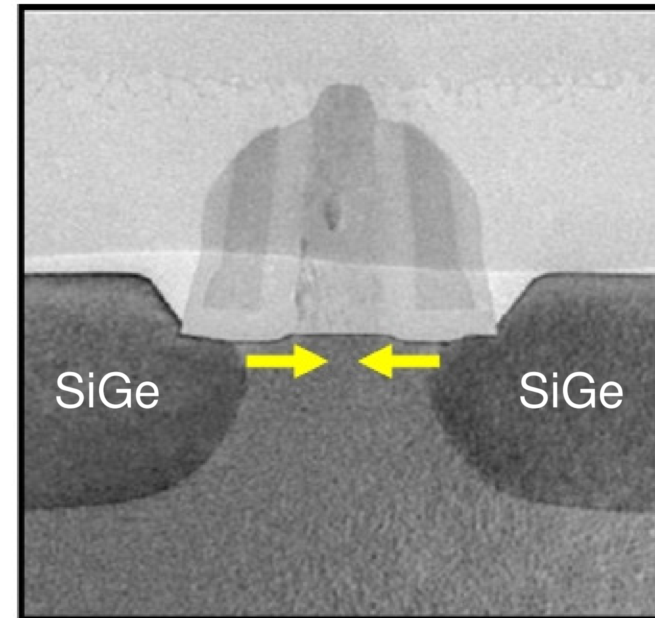
90 nm Strained Silicon Transistors

NMOS



SiN cap layer
Tensile channel strain

PMOS



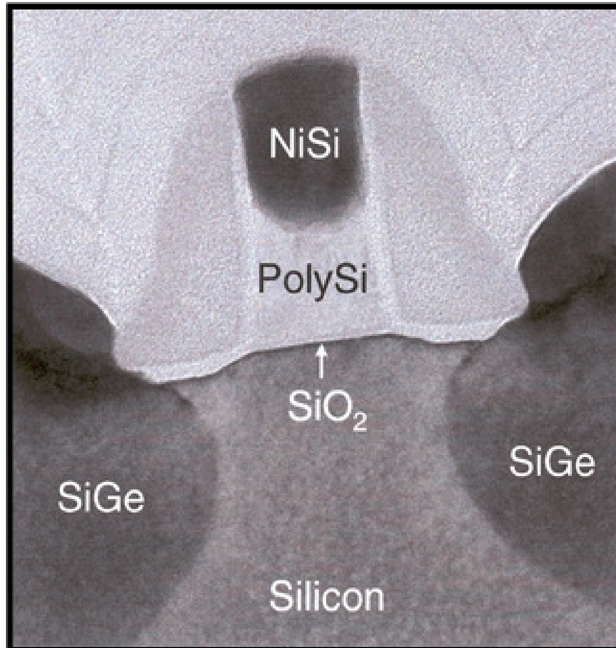
SiGe source-drain
Compressive channel strain

Strained silicon provided increased drive currents, making up for lack of gate oxide scaling

Mark Bohr, EE310 at Stanford 2011

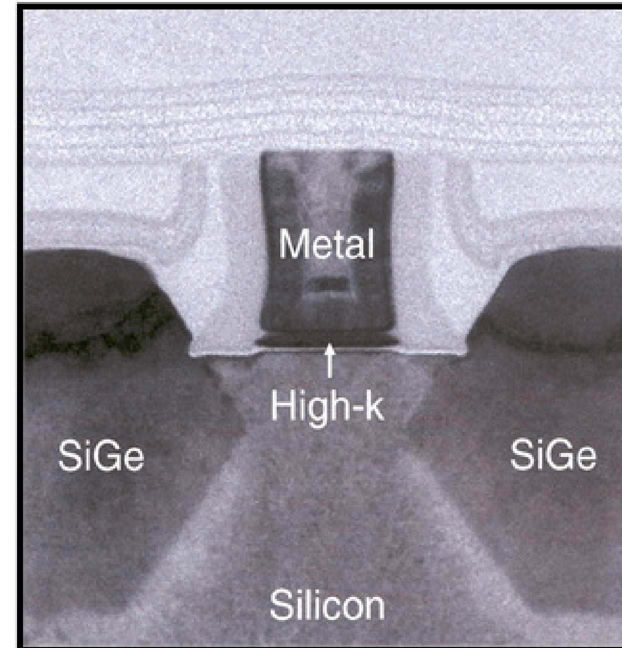
45 nm High-k Metal Gate Transistors

65 nm Transistor



SiO_2 dielectric
Polysilicon gate electrode

45 nm HK+MG

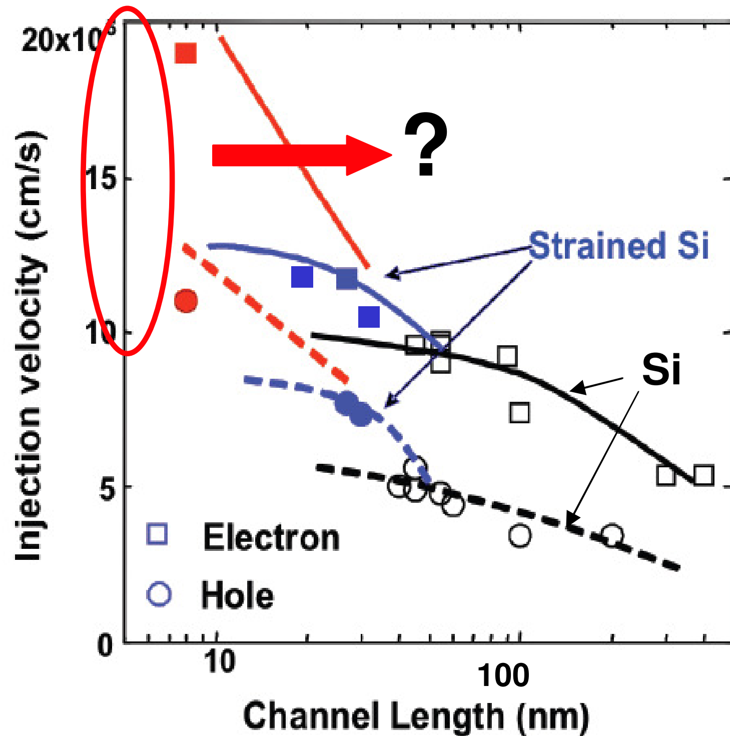


Hafnium-based dielectric
Metal gate electrode

High-k + metal gate transistors break through gate oxide scaling barrier

Mark Bohr, EE310, at Stanford, 2011

MOSFET geometry shrink is facing challenges…



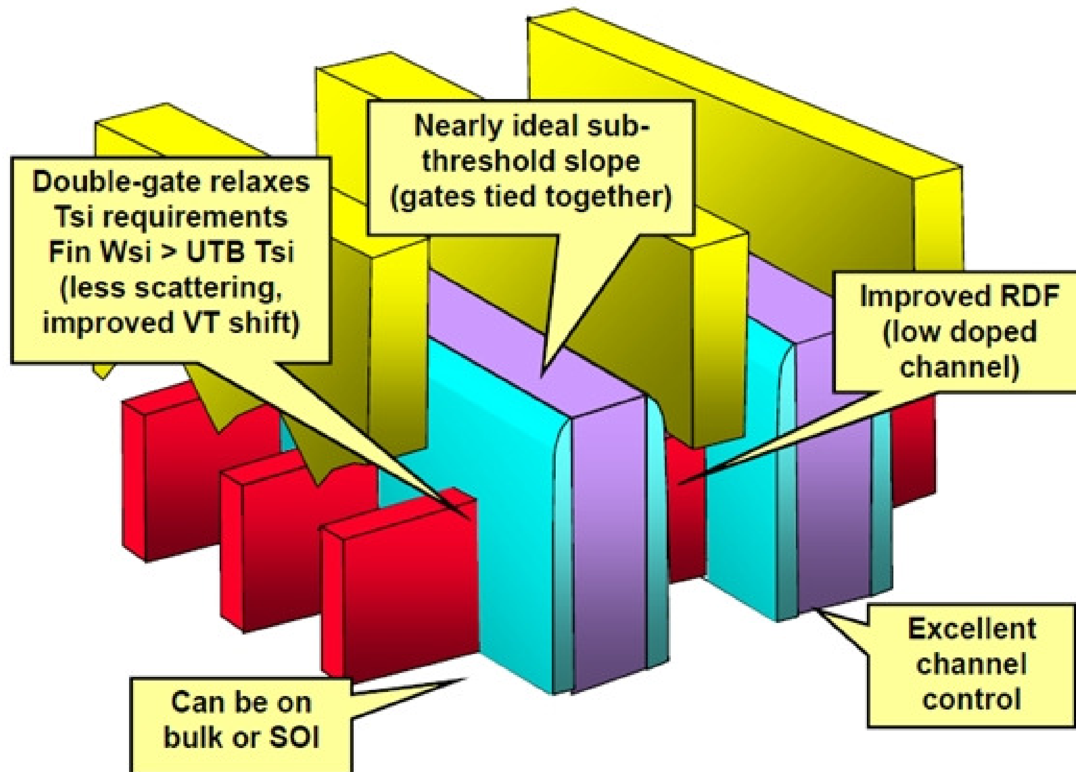
Courtesy: Prof. D. Antoniadis (MIT)

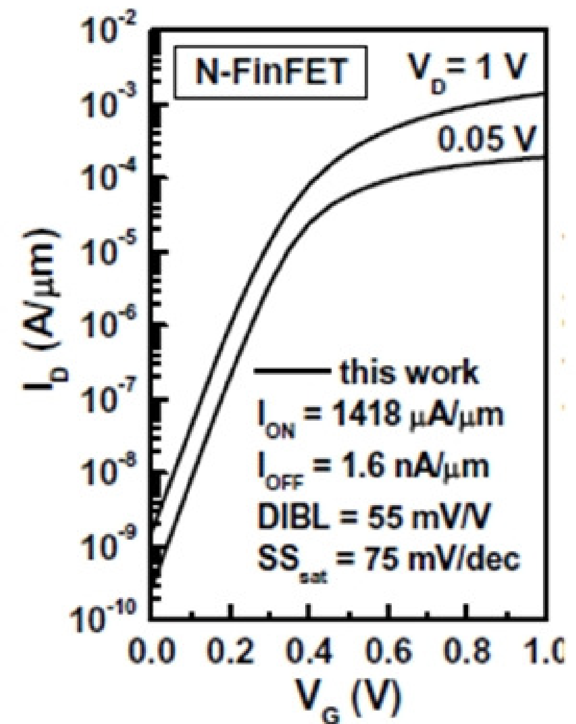
- **V_{inj} continued to increase with strained-Si technology, as if Si became a different material under strain.**
- **V_{inj} for sub 20nm should be much higher than strained-Si can give.**
- **High mobility channel:**
  Getting there (Lg=10nm) and proceeding beyond…

New channel material beyond strained Si

MuGFET Devices

Tri-Gate, FinFET





K. Kuhn, Intel, 2010

C-C Yeh, TSMC, IEDM 2010

Tomorrow

What's beyond scaling

- Logic devices: Non-silicon solution

  Germanium channel,

  III-V channel

  nano-wire, nanotube, nano-something

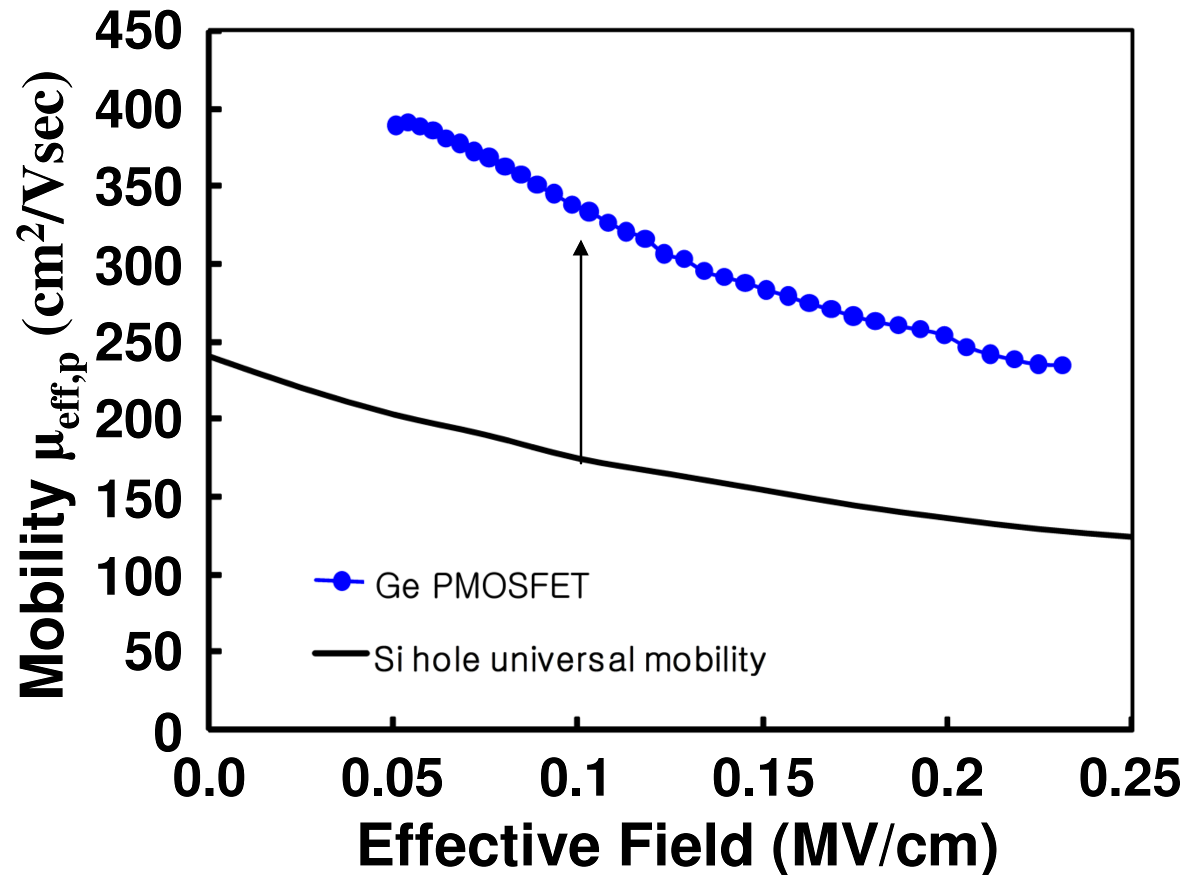
  graphene,

  topological insulator (?)
- Memory devices: New functional materials

  RRAM, PCRAM/polymer memory,

  STTRAM

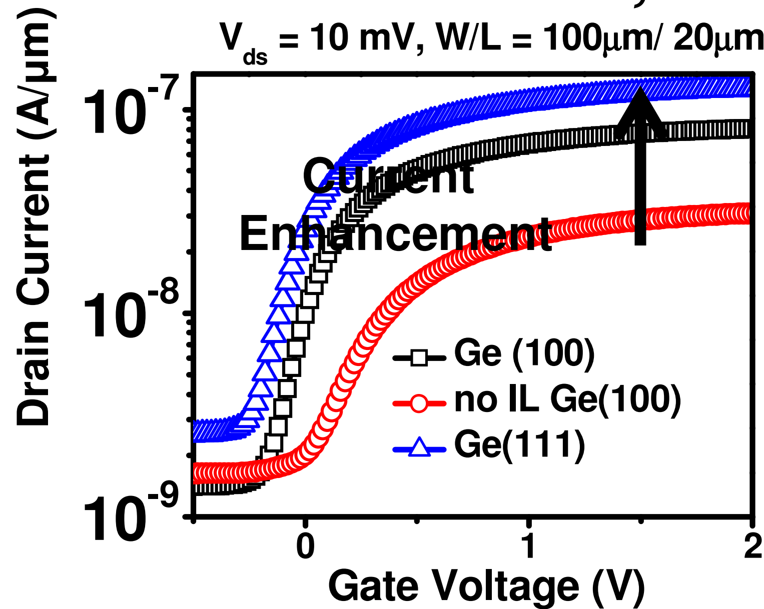
Ge PMOSFETs

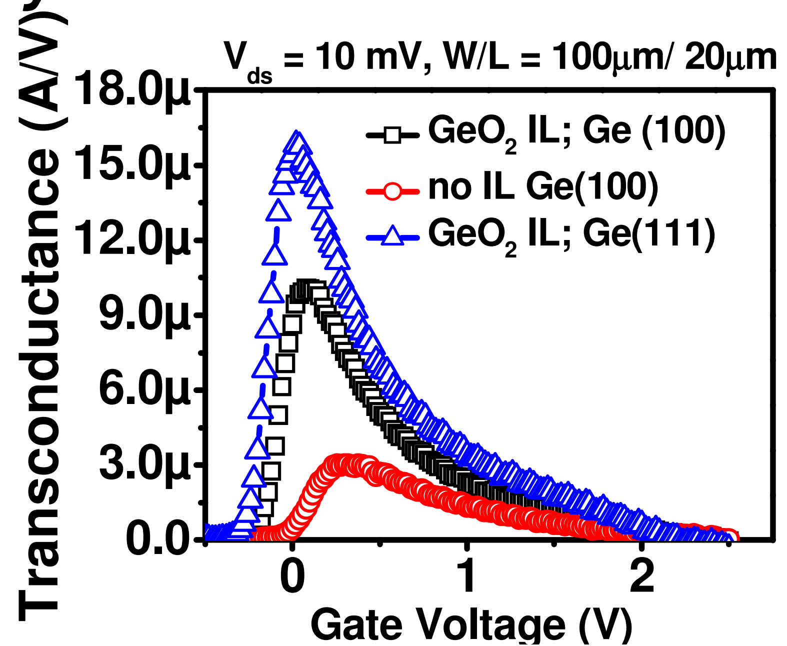


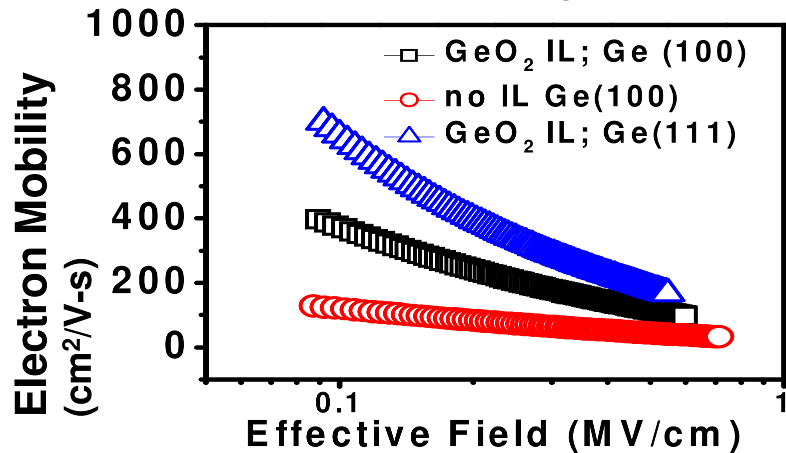
- **~80% mobility enhancement over Si universal mobility**

NMOSFETs?

Drive Current, Mobility Enhancement





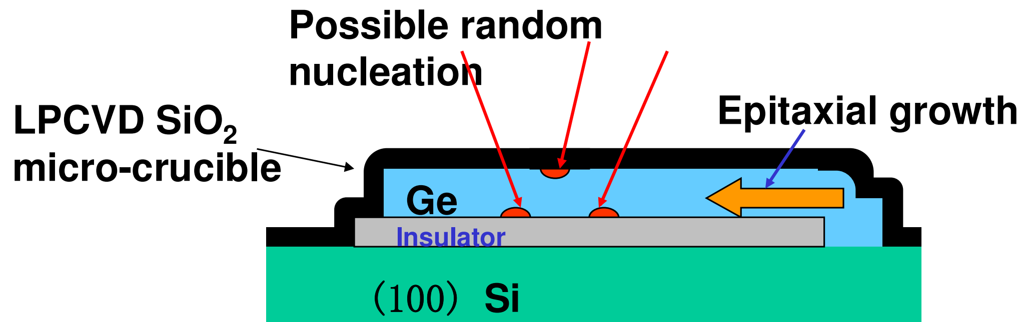


Ge(111) has higher mobility – lower m*
Samples without GeO_2 – poor mobility - interface/coulomb scattering..
EOT trade off

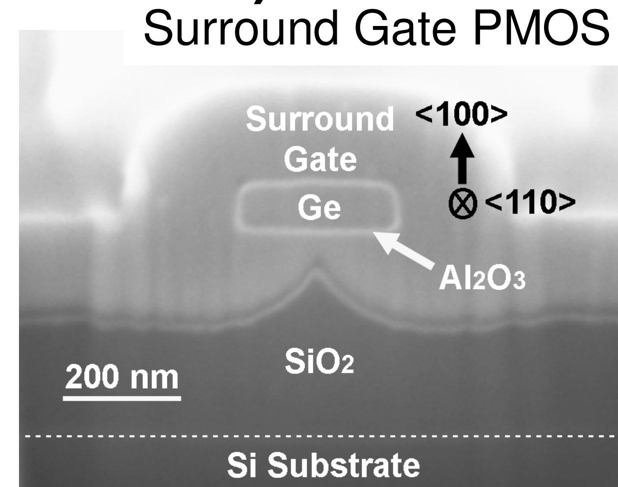
[1] **G.Thareja et al.,** Elec. Dev. Let. **32** (2011)608

Rapid Melt Growth Method for GeOI

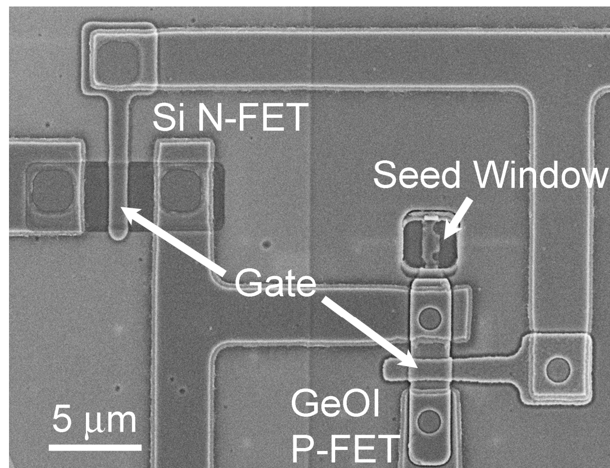
J. D. Plummer (Stanford)

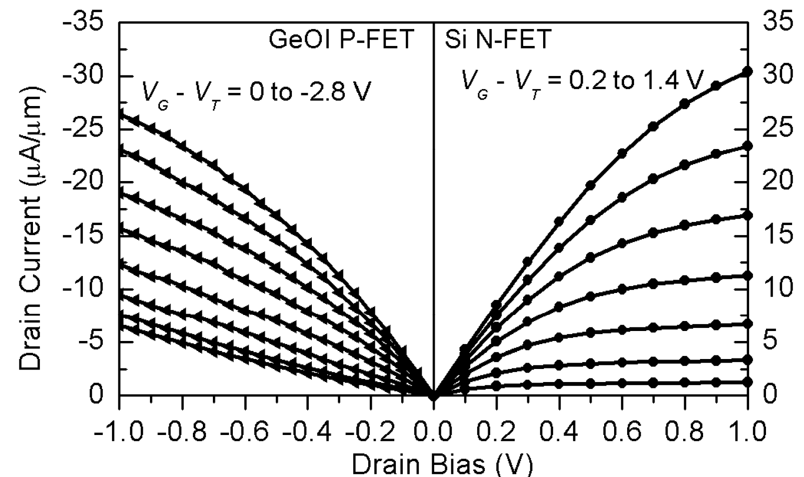


Surround Gate PMOS



Integration of Si NMOS and GeOI PMOS

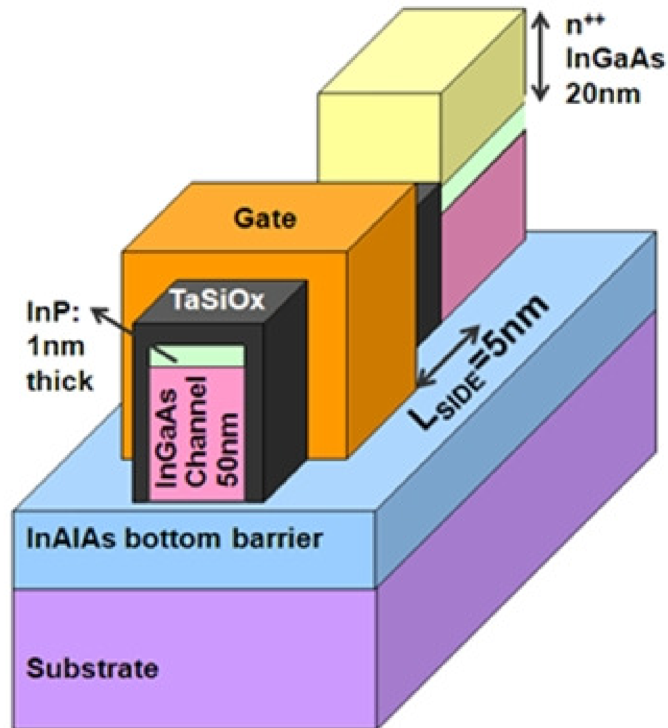


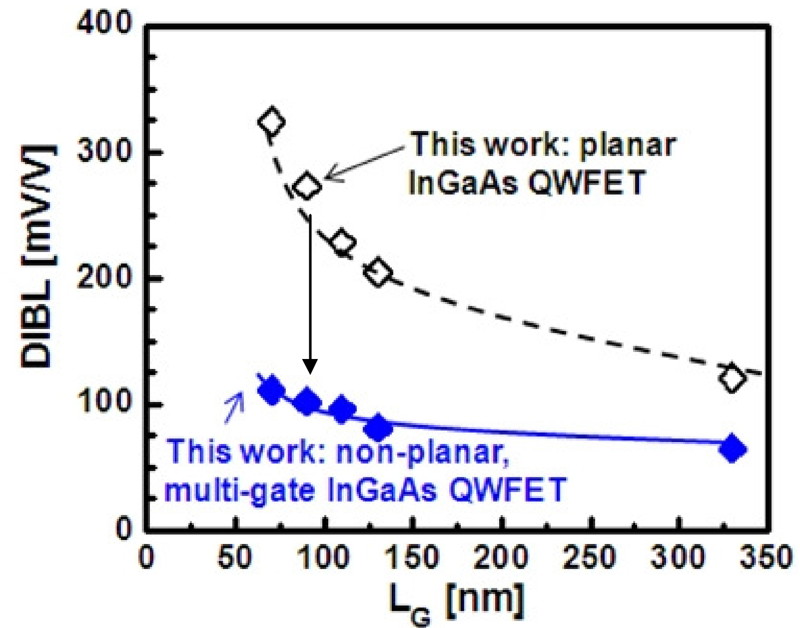


Rapid melt growth of Ge in micro-crucible from seed window shows high crystal quality GeOI devices

J. Feng et al, *IEEE Electron Device Lett.* (2006 & 2008)

III-V Transistor Options with DIBL improvement





M. Radosavljevic, Intel, IEDM 2010

If the future were to be in Heterogeneous Structures for CMOS Devices

Active Device Channel:

- Si nMOS with strain + Ge pMOS w or w/o strain
- Ge CMOS w or w/o strain
- III-V nMOS + Ge pMOS
- III-V nMOS + III-V pMOS with strain

On-chip Interconnect:

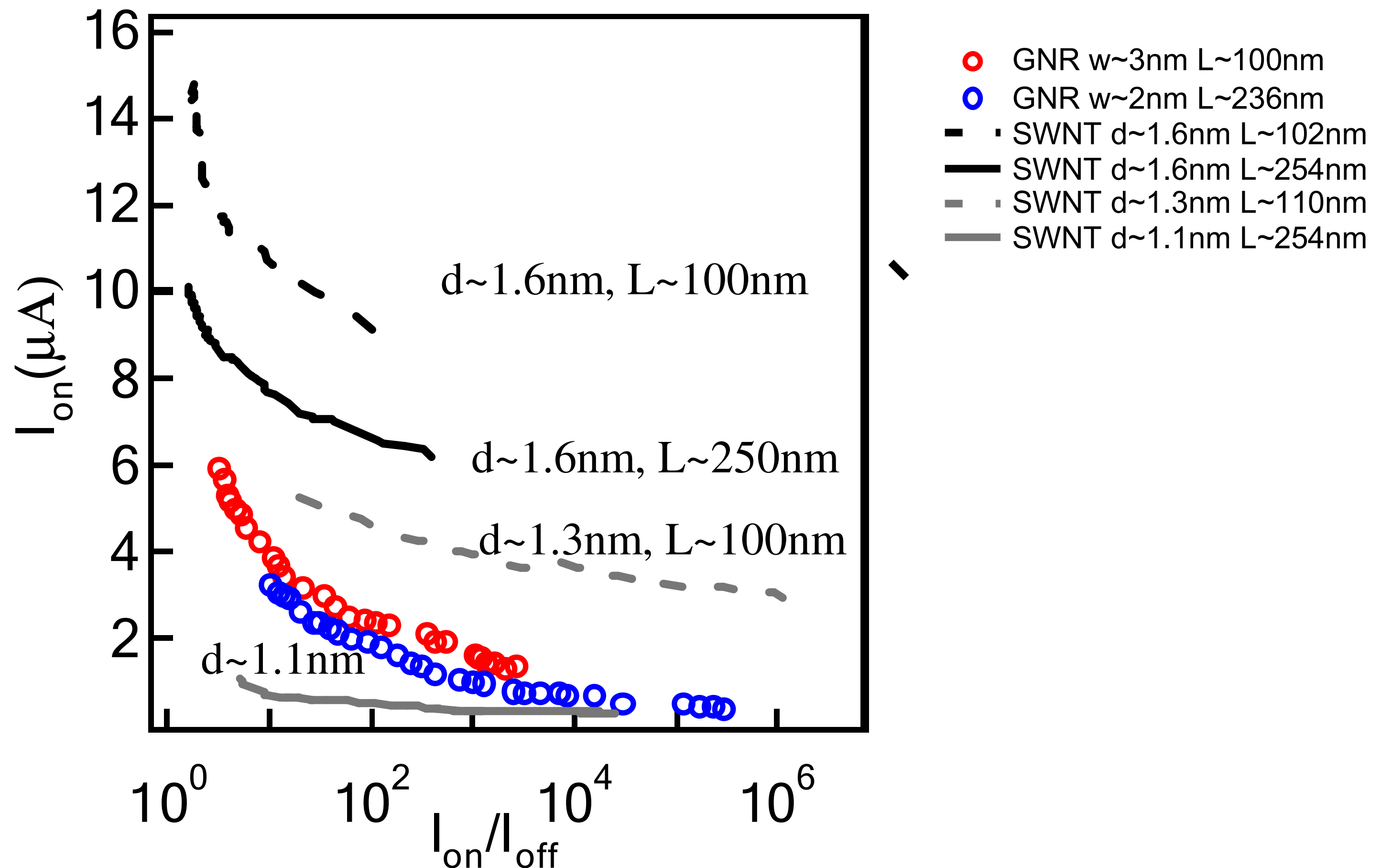
- Electrical + optical

Non-silicon high mobility channel approaches

- It will fulfill the needs for "higher speed and lower power consumption"
- High mobility materials-gate insulator interface is the biggest issue
- Ge option may provide an opportunity for on-chip optical interconnect; at least for detector, and maybe for transmitter if Ge laser is realized
- Integration density should stay with Si VLSI trend line (ITRS)??
- Preferential application on top of the Si platform looks rational option to go

Question: "What is the barrier which can rationalize such changes?"

Graphene ribbon vs. Carbon Nanotube



- ❖ High on/off GNR comparable to~1.2nm SWNT FETs
- ❖ GNR FETs comparable to high performance SWNT FETs (d~1.4-1.5nm) remains illusive

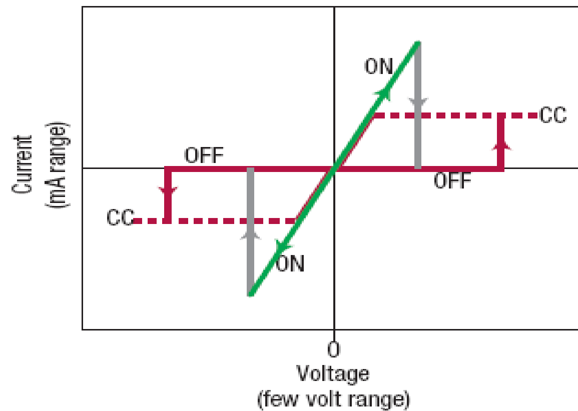
H. Dai, Stanford, 08

New Functional memory Opportunities

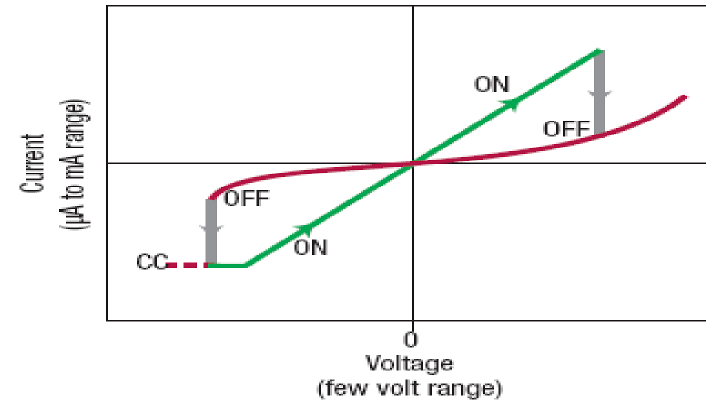
- Resistive switching
  - Transition metal oxides
  - Perovskites
  - Conductive bridges in solid state electrolytes
- Phase change
- Spin torque transfer
- Polymer…

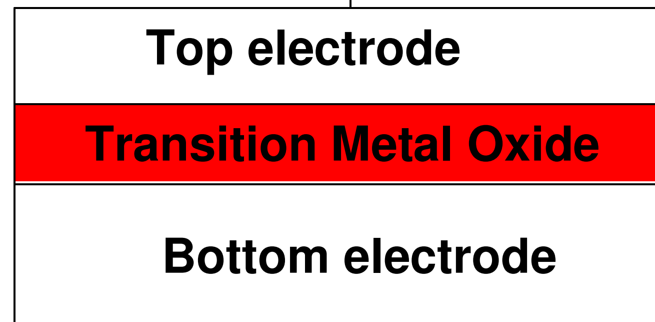
RRAM Switching Operation Polarity

Unipolar



Bipolar

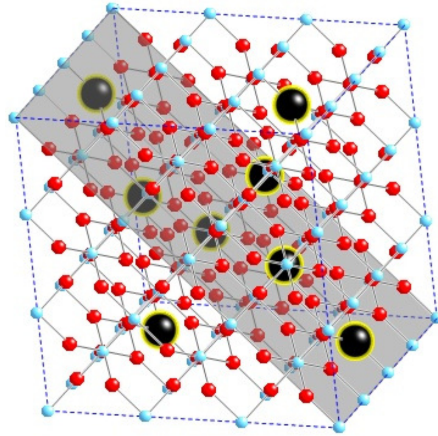


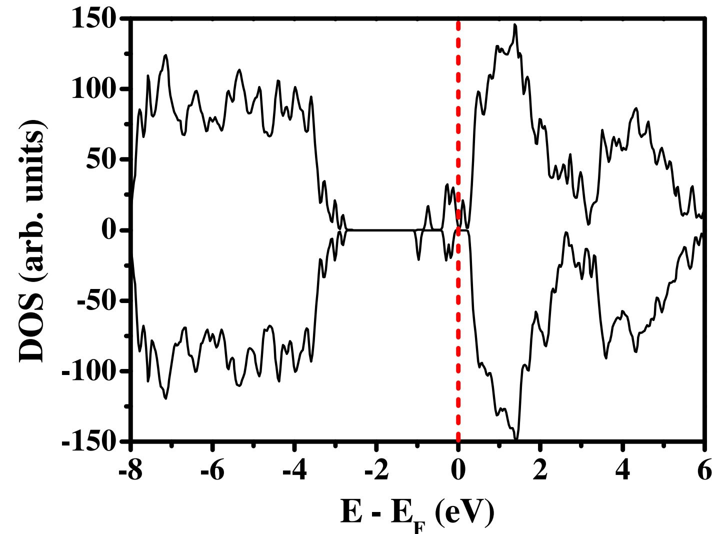


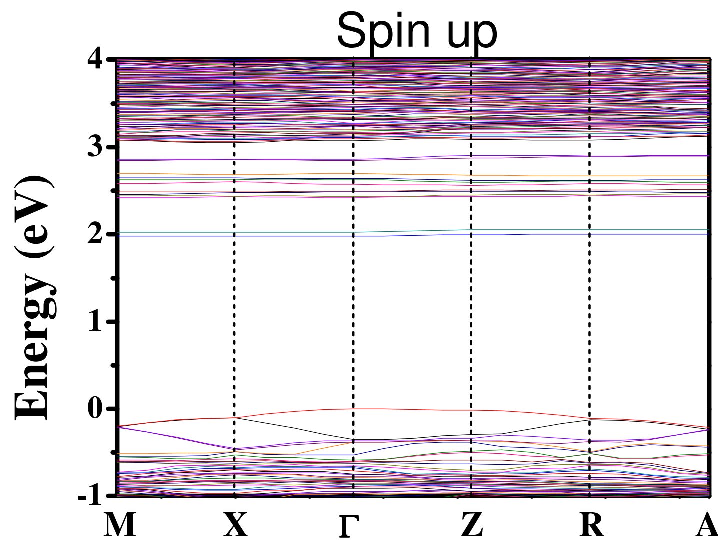
Ab-initio modeling/simulation approach to What is the conduction mechanism for the "on" state?

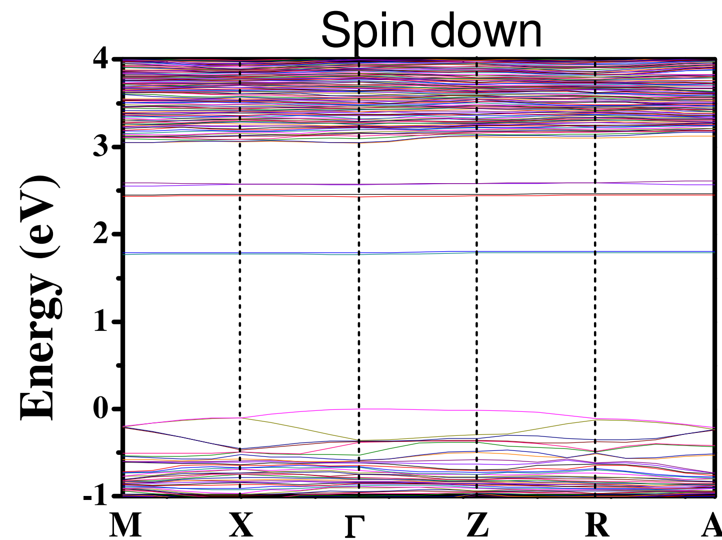
- Metallic filament?
- Vacancy chain?
- Local density of states arising from vacancy distribution or metallic behavior?
- Transport, electronic or ionic?
- Formation energy of conductive path?
- Macroscopic model vs atomic scale model?

Randomly Distributed Vacancies





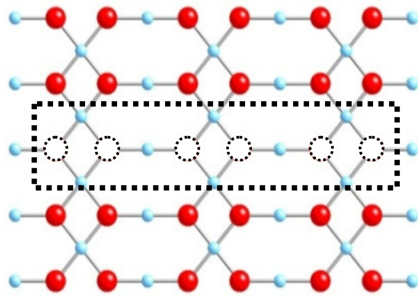


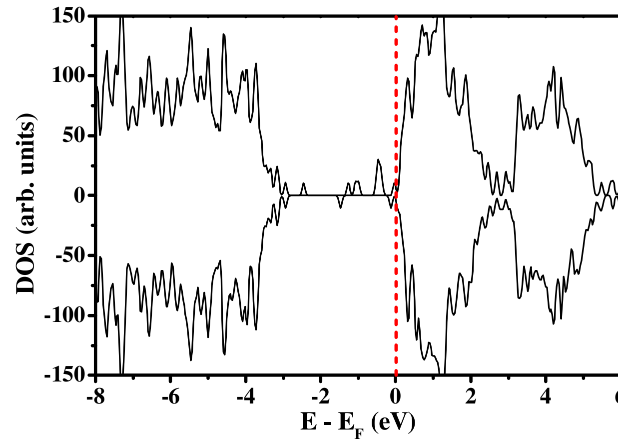


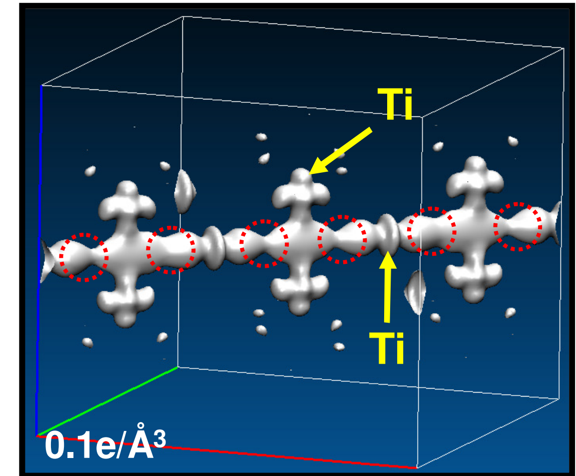
- **Even though we have more vacancies, lowering resistance is not so big as long as vacancies are randomly distributed.**

Ordering of Vacancies

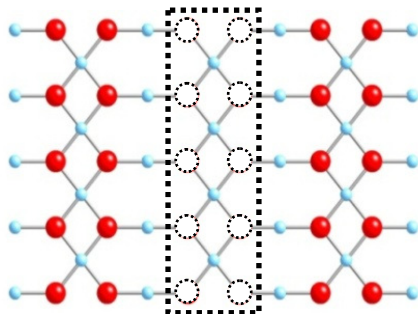
[110]



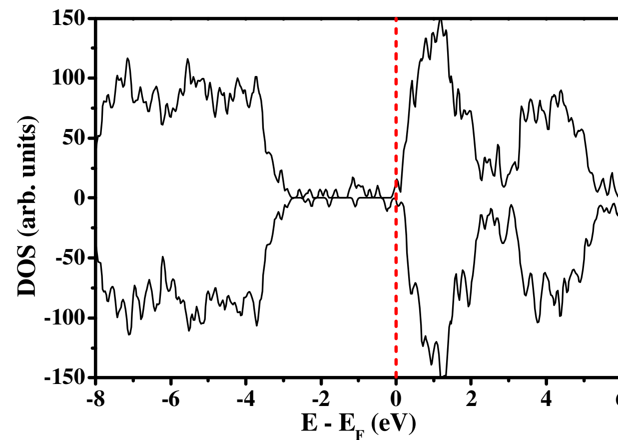


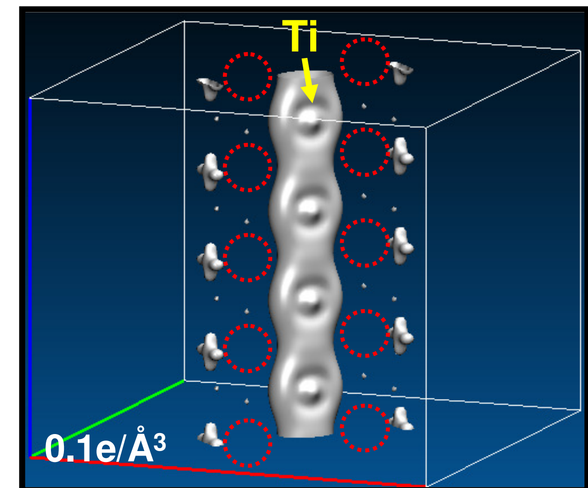


[001]



On –state





S.G. Park et al., EDL, 32, 197 (2011)

- **Filament type conductive channel which is composed of Ti atoms can be formed in either [001] or [110] direction.**

Stability of Vacancy Ordering

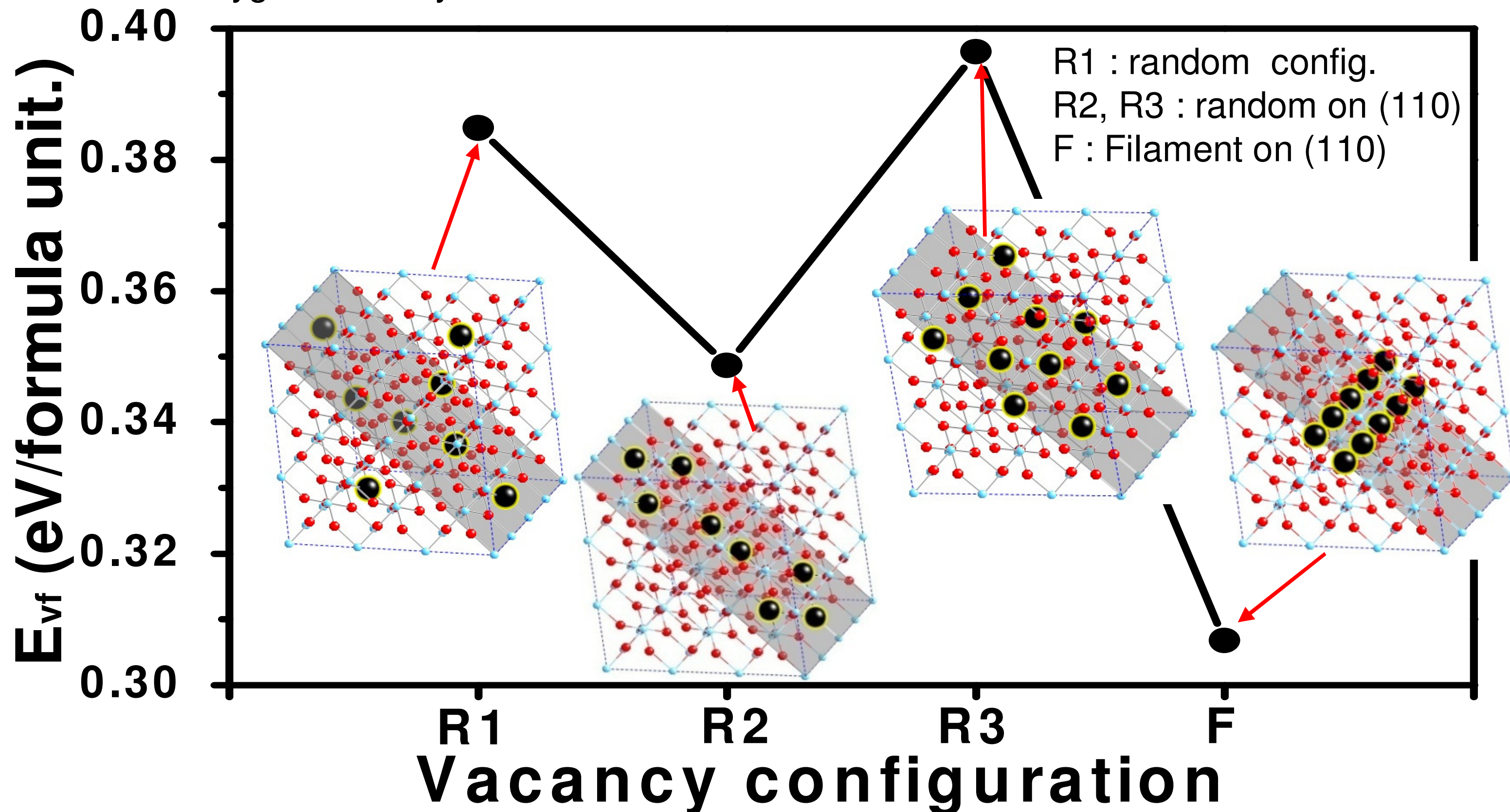
$$E_{vf} = E(TiO_{2-x}) - E(TiO_2) + n/2E(O_2)$$

$E(TiO_{2-x})$: The total energy of a supercell containing oxygen vacancies

$E(TiO_2)$: The total energy of a perfect TiO_2 in the same size of supercell

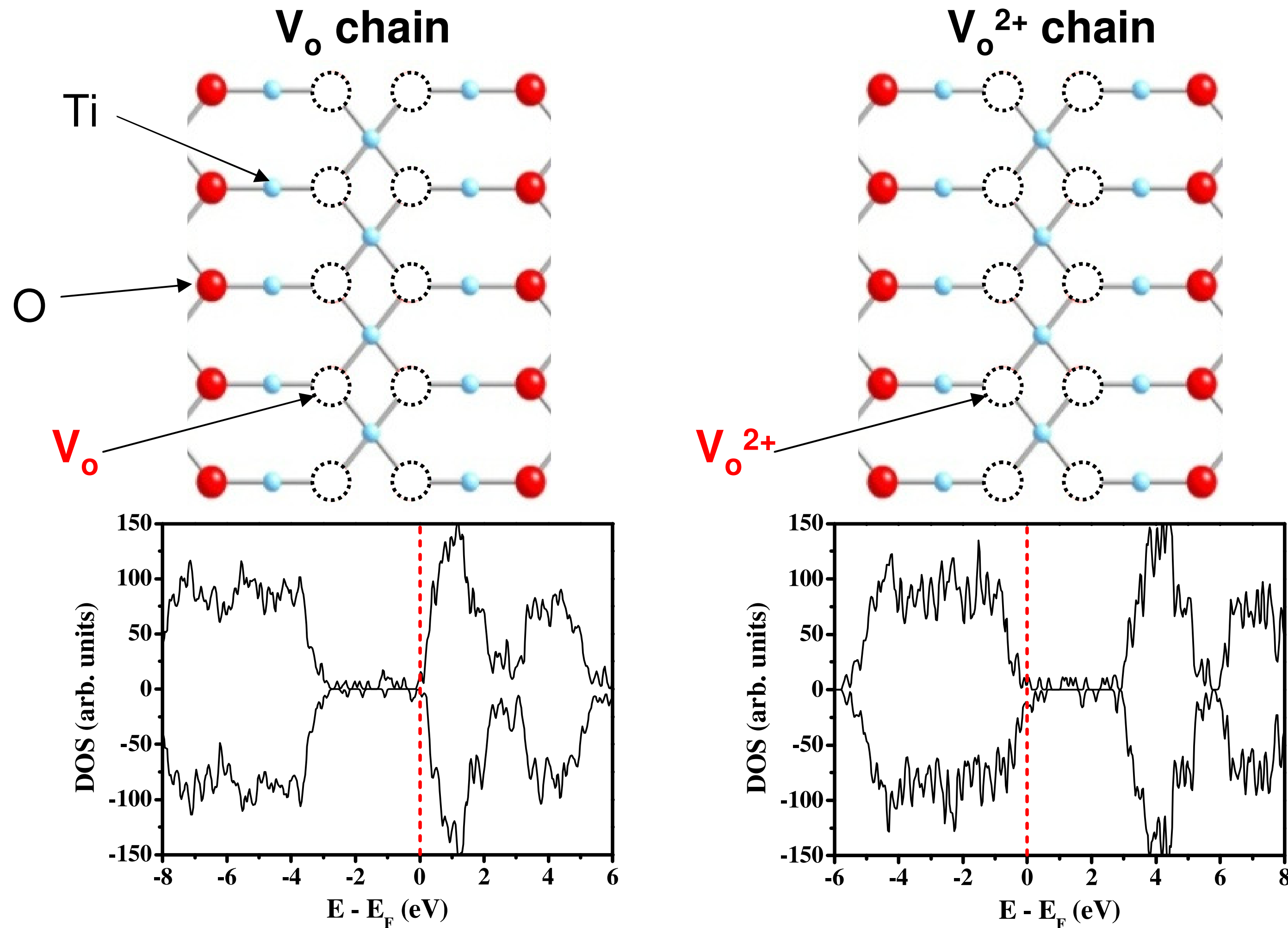
$E(O_2)$: The energy of oxygen molecule

n : The number of oxygen vacancy



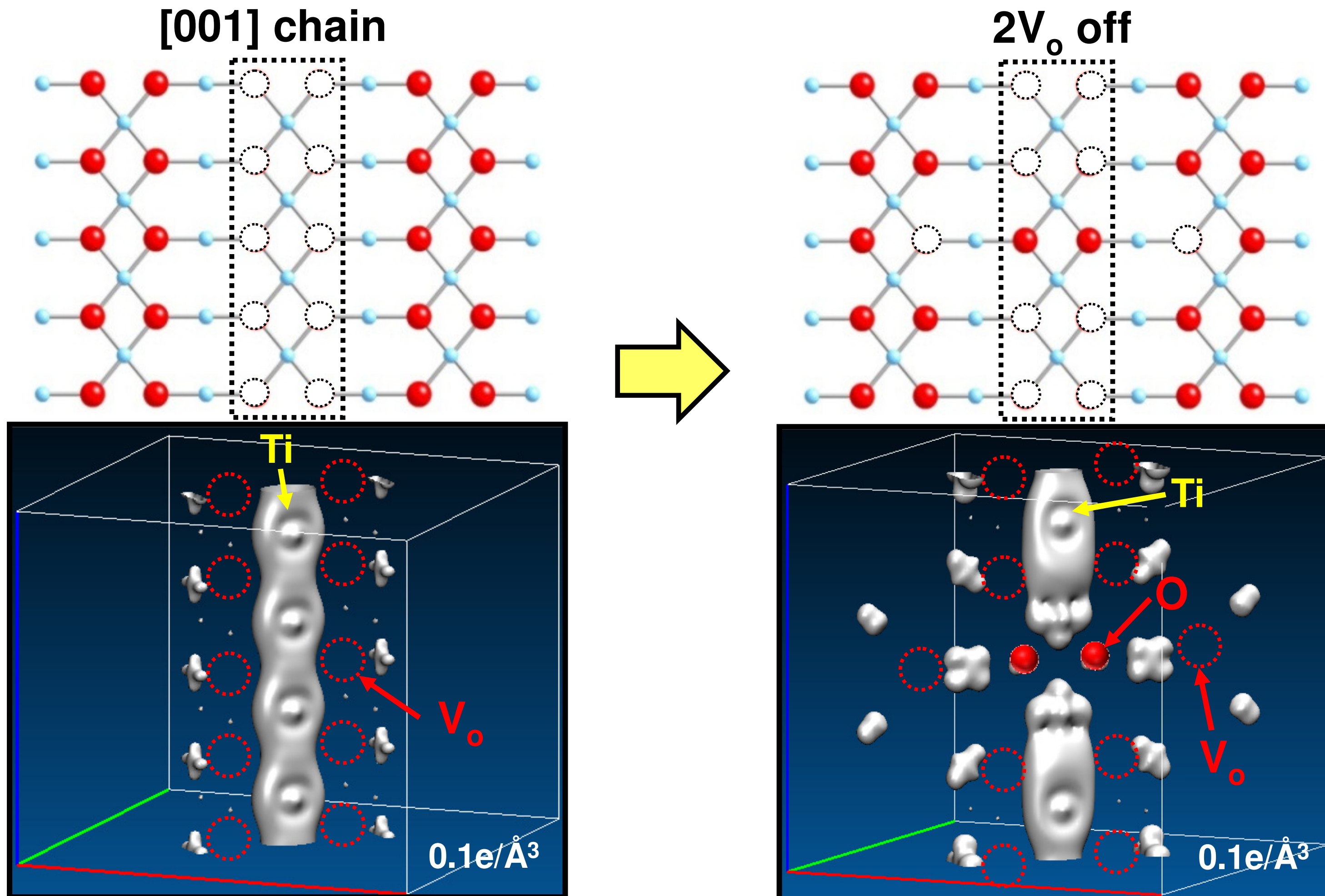
S.G. Park et al., EDL, 32, 197 (2011)

Charged Vacancy (V_o^{2+})



- **Even though electrons are removed from vacancies, many defect levels are still in the band gap with strong interactions.**

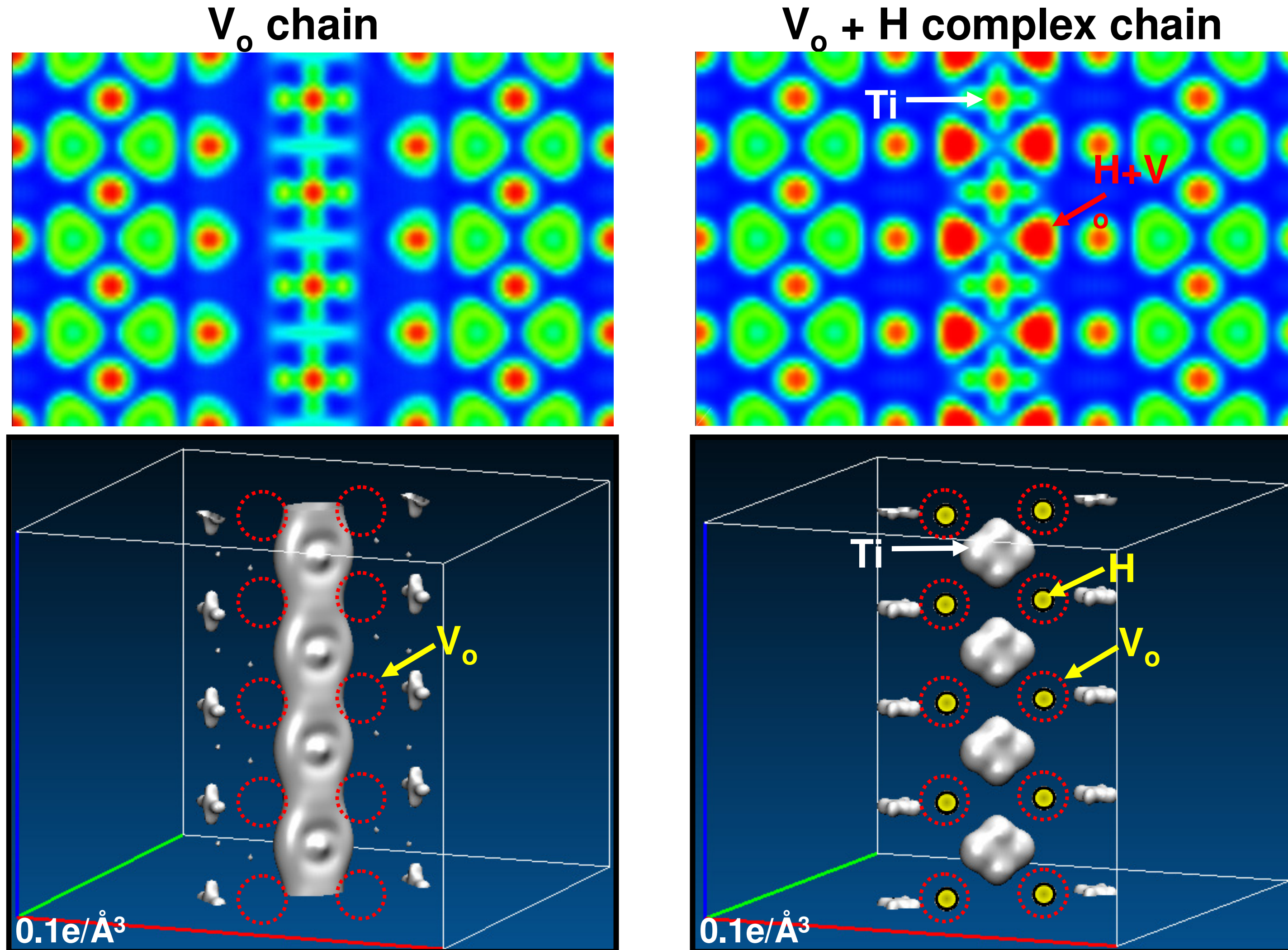
Rupture of Conductive Channel



S.G. Park et al., VLSI (2011), Kyoto, Japan

- **The conductive channel is disconnected by the diffusion of oxygen into the channel.**

Hydrogen in Conductive Channel

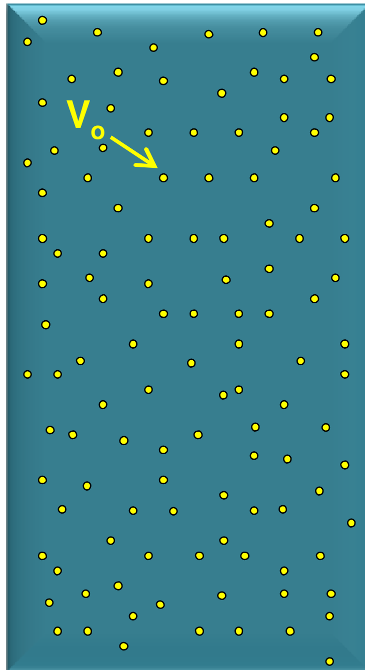


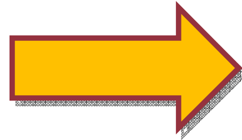
S.G. Park et al., VLSI (2011) (accepted)

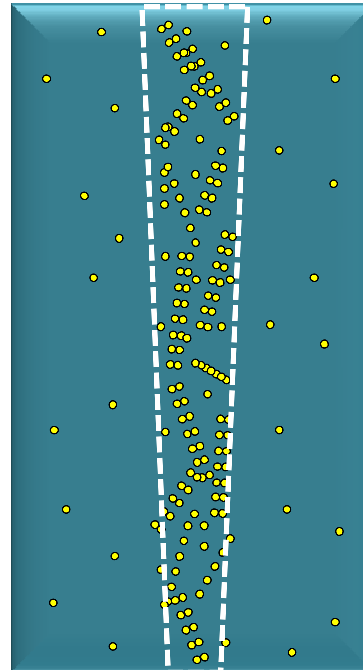
- **Hydrogen segregated to the vacancy sites - results in the rupture of the conductive channel by localizing electrons in those sites.**

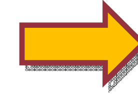
Switching Modeling

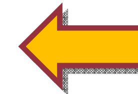
Initial (Insulator) **On (LRS)** **Off (HRS)**

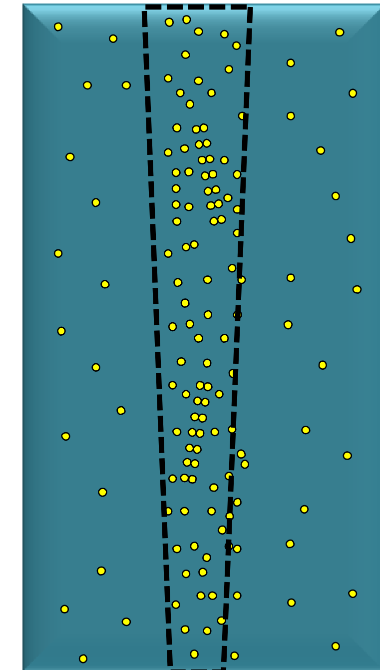












Vacancies in random **V_o ordered domains** **Disruption of V_o ordering**

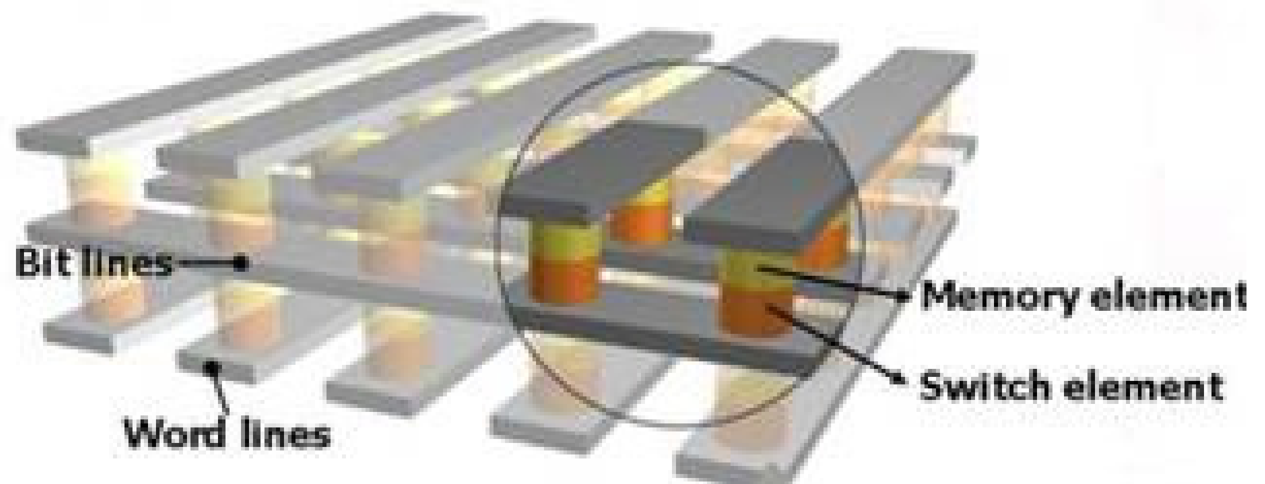
- **V_o concentration Increases locally → V_o are ordered. (LRS)**
- **Thermal heating by high current density → V_o diffuse out (HRS)**
- **The resistance of each state might be determined by the amount of vacancy ordered domains. (It doesn't have to be Magneli phase.)**

Vision for Memory Cell Confuguration

Concept: nonvolatile resistive-switching memory

Advantages:

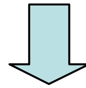
+ $4F^2$
+ 3D
+ MLC
+ Low cost
+ Fast (<1 μs)



Concerns: scaling (reset current) and reliability (data retention, noise, switching variability)

Paradigm Change in Emerging Memory Devices

- *Electrons and holes in stable structures of Si*



- *Electrons and holes in unstable structures*

  ions, vacancies, structural polarizations etc

- **Flood gate opened for new materials with new understanding and knowledge required**

  chalcogenides, perovskite, binary metal oxide, ferromagnetics, ferroelectrics, organic materials, carbon base materials etc

Metal Oxide RRAM (IEDM/VLSI) 2004-2010

	NiO IEDM 2004	Cu_xO IEDM 2005	Ti:NiO IEDM 2007	TaO_x IEDM 2008	HfO_x IEDM 2008	HfO_x IEDM 2009 &2010	WO_x IEDM 2010	WO_x IEDM 2010	GeO/HfON IEDM 2010	ZrO_x/HfO_x IEDM 2010
switching type	unipolar	bipolar	unipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar
Structure	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1R	1T-1R	1R	1R
cell Area (um^2)	~0.2	~0.03	~0.49	~0.25	~0.1	0.0009 (30nm)	8.1E-5 (9nm)	0.0036 (60nm)	11300	0.0025 (50nm)
speed	~5us	~50ns	~5ns	~10ns	~5ns	~300ps	~1us	~50ns	~20ns	~40ns
peak Voltage	<3V	<3V	<3V	<2V	<1.5V	<2.5V	<4V	<3V	<3V	<2V
peak Current	~2mA	~45uA	~100uA	~170uA	~25uA	~200uA	~1uA	~1mA	~0.1uA	~50 uA
HRS/LRS Ratio	>10	>10	>90	>10	>1,000	>1000	>10	>10	>700	>10
endurance	10^6	600	100	10^9	10^6	10^{10}	200	10^6	10^6	10^6
retention	300h@ 150℃	30h@ 90℃	1000h@ 150℃	3000h @ 150℃	10h@ 200℃	28h@ 150℃	280h temp. N/A	2000h @150 ℃	3h@125℃	28h@125℃

H.-S. P. Wong *et al.*, “Metal Oxide RRAM,” *Proc. IEEE*, 2011

Key enabler - new materials for NVRAM

- Yesterday
- Today or in view
- Under investigation

IA	IIA	IIIB	IVB	VB	VIB	VIIB	VIII			IB	IIB	IIIA	IVA	VA	VIA	VIIA	VIIIA
1 H 1.008																	2 He 4.003
3 Li 6.941	4 Be 9.012											5 B 10.81	6 C 12.01	7 N 14.01	8 O 16	9 F 19	10 Ne 20.18
11 Na 22.99	12 Mg 24.31											13 Al 26.98	14 Si 28.09	15 P 30.97	16 S 32.07	17 Cl 35.45	18 Ar 39.95
19 K 39.1	20 Ca 40.08	21 Sc 44.96	22 Ti 47.88	23 V 50.94	24 Cr 52	25 Mn 54.94	26 Fe 55.85	27 Co 58.47	28 Ni 58.69	29 Cu 63.55	30 Zn 65.39	31 Ga 69.72	32 Ge 72.59	33 As 74.92	34 Se 78.96	35 Br 79.9	36 Kr 83.8
37 Rb 85.47	38 Sr 87.62	39 Y 88.91	40 Zr 91.22	41 Nb 92.91	42 Mo 95.94	43 Tc -98	44 Ru 101.1	45 Rh 102.9	46 Pd 106.4	47 Ag 107.9	48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8	52 Te 127.6	53 I 126.9	54 Xe 131.3
55 Cs 132.9	56 Ba 137.3	57 La* 138.9	72 Hf 178.5	73 Ta 180.9	74 W 183.9	75 Re 186.2	76 Os 190.2	77 Ir 190.2	78 Pt 195.1	79 Au 197	80 Hg 200.5	81 Tl 204.4	82 Pb 207.2	83 Bi 209	84 Po -210	85 At -210	86 Rn -222
87 Fr -220	88 Ra -226	89 Ac** -227	104 Rf -257	105 Db -260	106 Sg -263	107 Bh -262	108 Hs -265	109 Mt -266	110 --- ()	111 --- ()	112 --- ()		114 --- ()		116 --- ()		118 --- ()

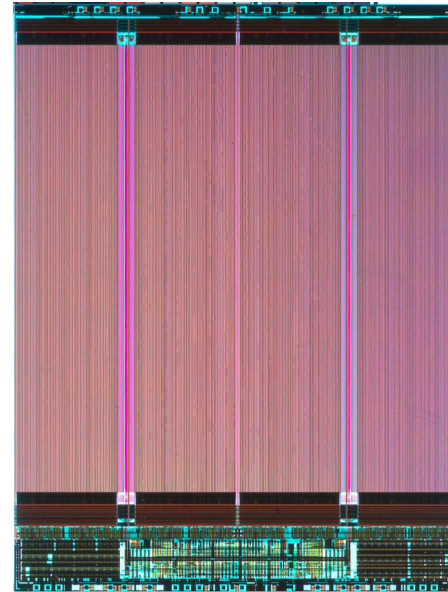
*	58 Ce 140.1	59 Pr 140.9	60 Nd 144.2	61 Pm -147	62 Sm 150.4	63 Eu 152	64 Gd 157.3	65 Tb 158.9	66 Dy 162.5	67 Ho 164.9	68 Er 167.3	69 Tm 168.9	70 Yb 173	71 Lu 175
**	90 Th 232	91 Pa -231	92 U -238	93 Np -237	94 Pu -242	95 Am -243	96 Cm -247	97 Bk -247	98 Cf -249	99 Es -254	100 Fm -253	101 Md -256	102 No -254	103 Lr -257

After passing the test at “device” level..

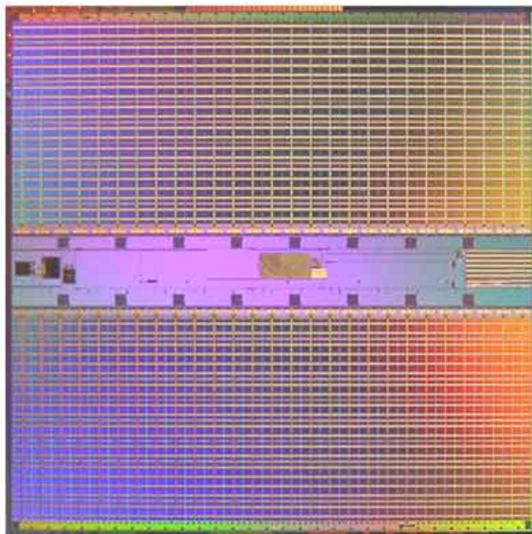
Integration!!

CMOS Technology Based Products in mid 2000s

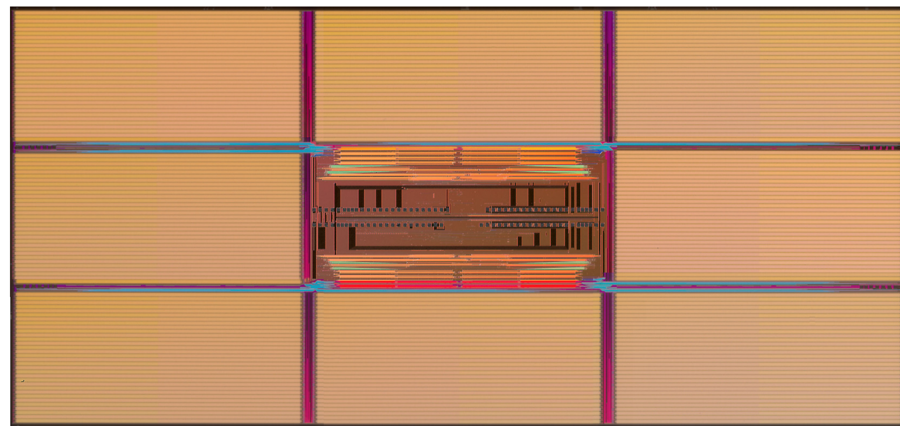
8Gb NAND, SAMSUNG



70 Mb SRAM, INTEL



2Gb DRAM, SAMSUNG



Likely "Road Block" for all of "nano" or "novel" materials

"Variability"

"Reproducibility"

"Integration"

Are we ready?? Perhaps "Not yet"!

However, this is not the first time……

MOSFET in early 60's

I can make the same numbers of PhDs as the number of MOSFETS I make!

This is a great toy for 2D quantization!

Integration!? No way!

Those are, however, in the situation where we had only Si, SiO2 and Al!

So, this is truly an exciting era for young bright people with tons of challenges ahead!

Technology & Topics in 60's

- Silicon replaced germanium, ***Ge again***
- Self-aligned silicon gate from Intel/Fairchild, ***Back to metal gate***
- Silicon VLS, ***Nanowires of Ge, III-V etc***
- Dielectric breakdown of insulators ***ReRAM***
- Ionic impurity in SiO_2 ***CBRAM***
- Ovonic devices became popular after their press release in '69, ***phase change memory***

New Technology & Topics in 70's

- Si CMOS, ***CMOS with non-silicon channel***
- SOS viewed as the major break though, ***SOI***
- Ovonic devices became popular after their press release in '69, ***phase change memory***
- Strained channel physics in SOS, ***Strained silicon MOS***
- Soft X-ray lithography and e-beam lithography, ***EUV lithography***
-

Future Technology Directions

More than Moore

CMOS

More Moore

Beyond CMOS

New Applications

Digital + analog + optical
Silicon + III-V
Electrical + Mechanical

New Technologies

Carbon Based?
Spintronics?
Magnetic Domains?
Molecular Switches?

2000 2010 2020 2030

New device technology will be needed by 2020

Mark Bohr, EE310 seminar at Stanford, 2011

Summary

- **Si as the dominant design in the past 3 decades because of cost/bit or logic superiority**
- **High speed switch may end up using non-silicon channel for better power-speed advantage, while traditional memory may be replaced with new material based nonvolatile memory *only if* they are integrated on silicon platform**
- **Potential road blocks**

  variability

  reproducibility

  integration

- Colleagues at Stanford: Krishna Saraswat, Philip Wong, Simon Wong, Paul McIntyre and Bruce Clemens for discussions and sharing some of their slides
- Friends in industry: Mark Bohr, Ghavam Shahidi, Hans Stork, M. Brillout
- Nishi group students and research staff members

INMP, NMTRI, CIS, MARCO, SRC, NSF, INTEL, IBM, TOSHIBA, TI, Samsung, Hynix, AMAT, TEL…